REMARKS

Claims 1 through 20 remain pending in the application. In response to the Office Action dated November 3, 2004, new drawing Fig. 20 is submitted herewith. The specification and claims 1and 20 have been amended. Care has been taken to avoid the introduction of new matter. Favorable reconsideration and allowance of the application are respectfully solicited.

Objection has been made to the drawings at paragraph 1 of the Office Action. The Office Action asserts that the drawings must show a first counter receiving said first initial value from said control circuit, adjusting a first count value to specify said oscillating cycle of said clock signal by using said first initial value as a first initial count value, and outputting said first count value, as recited in claim 1.

In response, it is submitted that these claim features indeed are illustrated in Fig. 2, which depicts digital counter 32 and phase 34 comparator. Delay line 30, OR gate 36, AND gate 38 and inverter Iv1 form a ring oscillator, as would be recognized by a person of ordinary skill in the art. Withdrawal of the objection is respectfully solicited.

Additional objection has been made to the drawings at paragraph 2 of the Office Action for lacking illustration of the fuse circuit, recited in claim 9, and the load circuit, recited in claim 19. In response, Fig. 20 has been submitted. Fig. 20 exemplifies a well known fuse storage circuit that corresponds to the storage unit 13, shown in block diagram form in Fig. 1. It is submitted that the original disclosure of the storage unit 13 in Fig. 1 and the specification description at page 18, line 20, that "it is possible to construct storage unit 13 by a fuse circuit," provides appropriate support in the original disclosure for Fig. 20. The addition of Fig. 20, therefore, does not present new matter. The configuration itself of the fuse circuit shown in Fig. 20 is conventional and is within the technical knowledge of a person of ordinary skill in the art.

Such a person would have recognized that the configuration as shown in Fig, 20 would be derived from the descriptions on page 18, lines 15-21 and page 25, lines 7-12 of the specification, which state that storage unit 13 may take the form of a fuse circuit that can be laser-trimmed. Amendment has been made to the specification to describe Fig. 20.

Claim 19 recites: "when a load capacity of a load circuit changes and, then, returns to the state before the change, said control circuit sets said count value read from said counter before the change as said initial value into said counter." The "load circuit" of claim 19 corresponds to the external circuit 180 illustrated in Fig. 19. Page 28, lines 5-28 of the specification, explain how the load capacity of external circuit 180 changes.

Withdrawal of the objection set forth in paragraph 2 of the Office Action is respectfully solicited.

Further objection has been made to the drawings at paragraph 3 of the Office Action. In response, it is noted that the counter, which forms the basis of the objection, corresponds to the digital counter 168, illustrated in Fig. 19. Withdrawal of the objection is respectfully solicited.

Claims 1 through 16 have been rejected under the first paragraph of 35 U. S. C. § 112. The Office Action purports that enabling disclosure is lacking for the features recited in claims 1 and 6 through 10. Claims 17 through 20 have been rejected under the first paragraph of 35 U. S. C. § 112 for lacking enabling disclosure. The rejections are respectfully traversed. It is submitted that Figs. 2 and 3 and the accompanying description thereof in the specification provide appropriate explanation to enable a person of ordinary skill in the art to understand to make and use the invention, as required by the statute.

The control circuit of claim 1 is described in detail in the specification as CPU 12, for example, at page 8, lines 4-16, and page 17, line 1 to page 18, line 8. "Setting a first initial value

in said clock generating circuit" finds enabling support in the specification descriptions, for example, at page 8, lines 4-16, and page 17, line 32 to page 18, line 4. "[O]n the basis of a first instruction from the outside" finds enabling support in the specification descriptions, for example, at page 17, lines 1-31 and page 16, lines 16-19.

The first counter, recited in claim 1, is described in detail as digital counter 32, for example, at page 9, lines 10-16, at page 12, line 7 to page 13, line 12, and page 17 line 32, to page 18, line 4 of the specification. "[U]sing said first initial value as a first initial count value" finds enabling support at page 17, line 32 to page 18, line 4 of the specification. "[A]djusting a first count value to specify said oscillating cycle of said clock signal by using said first initial value as a first initial count value" finds enabling support in the description of explanation of the operations of multiplication circuit 20 on page 12, line 7, to page 13, line 12, of the specification.

The "detection circuit" and the "control circuit" recited in claims 6 through 8 are described in detail in the third embodiment. The "detection circuit" is described in detail on page 20, lines 22-32, as detection circuits 24, 24A shown in Figs. 15, 16. The "control circuit" is described in detail as CPU 12, on page 20, line 33 to page 21, line 7.

The "pulse counter", the "control circuit" and the "storage circuit" recited in claims 9 and 10 are described in detail in the fourth embodiment. The "pulse counter" is described in detail on page 23, lines 2-13, as pulse counter 60 shown in Fig. 17. The "control circuit" is described in detail on page 23, line 14 to page 24, line 12, as CPU 12 shown in Fig. 17. The "storage circuit" is described in detail as storage unit 13 shown in Fig. 17.

The "counter" recited in claim 17 is described on page 25, line 28 to page 26, line 7 as digital counter 168 in the fifth embodiment. "[A]djusting a count value to specify a delay

amount of said first clock signal by using said initial value as a first initial count value on the basis of said phase comparison result, and outputting said adjusted count value" is described for example on page 26, lines 1-7, page 26, line 28 to page 27, line 3, and page 27, lines 14-21 of the specification.

The "load circuit" recited in claim 19 is described in detail on page 28, lines 5-28, as external circuit 180 in the fifth embodiment.

It is submitted that a person of ordinary skill in the, from the above identified portions of the disclosure, would have been able to understand, implement and use the invention recited in claims 1 through 20. Withdrawal of the rejections is respectfully solicited.

Claims 1 through 5 and 17 have been rejected further under 35 U. S. C. § 102(b) as being anticipated by U.S. patent 6,225,840 (Ishimi). The rejection is respectfully traversed.

Independent claim 1 has been amended to recite ,*inter alia*,

> said clock generating circuit includes a multiplication circuit, and said multiplication circuit includes:
>
> a first counter receiving said first initial value from said control circuit, adjusting a first count value to specify said oscillating cycle of said clock signal by using said first initial value as a first initial count value, and outputting said first count value; and
>
> an oscillation circuit receiving said first count value from said first counter and oscillating said clock signal on the basis of said first count value.

The Office Action reads the control circuit, the first counter and the oscillation circuit, recited in claim 1, respectively, on arithmetic unit 30, counter 31, and the circuit formed of the digital delay line 33 and the fixed delay circuit 34, that are inc1uded in the phase synchronous circuit 11 shown in Fig. 2 of Ishimi.

Ishimi, however, does not disclose or suggest the control circuit set a first initial value

in the clock generating circuit on the basis of a first instruction from the outside. An object of the present invention is to make it possible for a user of the information processing apparatus to properly and flexibly make settings of the PLL circuit, as described on page 3, lines 19-29 of the specification. To achieve this object, according to the invention recited in claims 1 and 17, the control circuit sets the first initial value in the clock generating circuit "on the basis of Ii first instruction from the outside". This means that the count value (first initial value) is calculated according to a program that the user of the information processing apparatus can program, as described on page 16, lines 16-19 of the specification. No such operation is disclosed or suggested by Ishimi.

Claims 6 through 16 and 18 through 20 have not been rejected on the basis of prior art.

Withdrawal of all objections and rejections, and allowance of the application, are respectfully solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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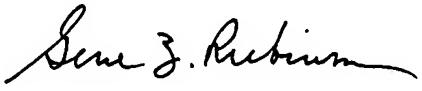

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